

CLAIMS

What is claimed is:

- 1) A triple redundant latch for reducing soft errors comprising:
 - a) a first settable memory element;
 - b) a second settable memory element;
 - c) a third settable memory element;
 - d) a voting structure;
 - e) wherein an identical logic value is set in each settable memory element;
 - f) wherein the voting structure determines a logical value held on the third settable memory element after the first, second, and third settable memory elements are set;
 - g) wherein inputs to the voting structure are provided by the first settable memory element, the second settable memory element, and control signals used to set the settable memory elements;
 - h) wherein a propagation delay through the third settable memory element is the only propagation delay of the triple redundant latch.
- 2) The triple redundant latch as in Claim 1 wherein the first settable memory element comprises:
 - a) a transfer gate and;
 - b) a latch.

- 3) The triple redundant latch as in Claim 2 wherein the transfer gate consists of a complementary pass gate.
- 4) The triple redundant latch as in Claim 2 wherein the transfer gate consists of an NFET-only pass gate.
- 5) The triple redundant latch as in Claim 2 wherein the transfer gate consists of a PFET-only pass gate.
- 6) The triple redundant latch as in Claim 1 wherein the second settable memory element comprises:
 - a) a transfer gate and;
 - b) a latch.
- 7) The triple redundant latch as in Claim 6 wherein the transfer gate consists of a complementary pass gate.
- 8) The triple redundant latch as in Claim 6 wherein the transfer gate consists of an NFET-only pass gate.
- 9) The triple redundant latch as in Claim 6 wherein the transfer gate consists of a PFET-only pass gate.
- 10) The triple redundant latch as in Claim 1 wherein the third settable memory element comprises:

- a) a transfer gate and;
- b) a latch.

11) The triple redundant latch as in Claim 10 wherein the transfer gate consists of a complementary pass gate.

12) The triple redundant latch as in Claim 10 wherein the transfer gate consists of an NFET-only pass gate.

13) The triple redundant latch as in Claim 10 wherein the transfer gate consists of a PFET-only pass gate.

14) A triple redundant latch for reducing soft errors comprising:

- a) a first transfer gate, the first transfer gate having an input, a first control input, a second control input, and an output;
- b) a second transfer gate, the second transfer gate having an input, a first control input, a second control input, and an output;
- c) a third transfer gate, the transfer third gate having an input, a first control input, a second control input and an output;
- d) a first latch, the first latch having an input and an output;
- e) a second latch, the second latch having an input and an output;
- f) a third latch, the third latch having an input/output;
- g) a majority voter, the majority voter having a first input, a second input, a third input, fourth input, and an output;

- h) wherein the input of triple redundant latch is connected to the input of the first transfer gate, the input of the second transfer gate, and the input of the third transfer gate;
- i) wherein the output of the triple redundant latch is connected to the input/output of the third latch;
- j) wherein a first control input of the triple redundant latch is connected to the first control input of the first transfer gate, the first control input of the second transfer gate, the first control input of the third transfer gate, and the third input to the majority voter;
- k) wherein a second control input of the triple redundant latch is connected to the second control input of the first transfer gate, the second control input of the second transfer gate, the second control input of the third transfer gate, and the fourth input to the majority voter;
- l) wherein the output of the first transfer gate is connected to the input of the first latch;
- m) wherein the output of the second transfer gate is connected to the output of the majority voter, and the input/output of the third latch;
- n) wherein the output of the third transfer gate is connected to the input of the second latch;
- o) wherein the output of the first latch is connected to the first input of the majority voter;
- p) wherein the output of the second latch is connected to the second input of the majority voter.

15) The triple redundant latch as in Claim 14 wherein the first transfer gate comprises:

- a) a PFET, the PFET having a gate, a drain and a source;
- b) a NFET, the NFET having a gate, a drain and a source;
- c) wherein the drains of the PFET and the NFET are connected to the input of the first transfer gate;
- d) wherein the sources of the PFET and the NFET are connected to the output of the first transfer gate;
- e) wherein the gate of the NFET is connected to the first control input of the first transfer gate;
- f) wherein the gate of the PFET is connected to the second control input of the first transfer gate.

16) The triple redundant latch as in Claim 14 wherein the second transfer gate comprises:

- a) a PFET, the PFET having a gate, a drain and a source;
- b) a NFET, the NFET having a gate, a drain and a source;
- c) wherein the drains of the PFET and the NFET are connected to the input of the second transfer gate;
- d) wherein the sources of the PFET and the NFET are connected to the output of the second transfer gate;
- e) wherein the gate of the NFET is connected to the first control input of the second transfer gate;
- f) wherein the gate of the PFET is connected to the second control input of the second transfer gate.

17) The triple redundant latch as in Claim 14 wherein the third transfer gate comprises:

- a) a PFET, the PFET having a gate, a drain and a source;
- b) a NFET, the NFET having a gate, a drain and a source;
- c) wherein the drains of the PFET and the NFET are connected to the input of the third transfer gate;
- d) wherein the sources of the PFET and the NFET are connected to the output of the third transfer gate;
- e) wherein the gate of the NFET is connected to the first control input of the third transfer gate;
- f) wherein the gate of the PFET is connected to the second control input of the third transfer gate.

18) The triple redundant latch as in Claim 14 wherein the first latch comprises:

- a) a first PFET, the first PFET having a gate, a drain and a source;
- b) a second PFET, the second PFET having a gate, a drain and a source;
- c) a first NFET, the first NFET having a gate, a drain and a source;
- d) a second NFET, the second NFET having a gate, a drain and a source;
- e) wherein the sources of the first and second PFETs are connected to VDD;
- f) wherein the sources of the first and second NFETs are connected to GND;

- g) wherein the gate of the first NFET, the gate of the first PFET, the drain of the second NFET, and the drain of the second PFET are the input of the first latch;
- h) wherein the drain of the first NFET, the drain of the first PFET, the gate of the second NFET, and the gate of the second PFET are the output of the first latch.

19) The triple redundant latch as in Claim 14 wherein the second latch comprises:

- a) a first PFET, the first PFET having a gate, a drain and a source;
- b) a second PFET, the second PFET having a gate, a drain and a source;
- c) a first NFET, the first NFET having a gate, a drain and a source;
- d) a second NFET, the second NFET having a gate, a drain and a source;
- e) wherein the sources of the first and second PFETs are connected to VDD;
- f) wherein the sources of the first and second NFETs are connected to GND;
- g) wherein the gate of the first NFET, the gate of the first PFET, the drain of the second NFET, and the drain of the second PFET are the input of the second latch;
- h) wherein the drain of the first NFET, the drain of the first PFET, the gate of the second NFET, and the gate of the second PFET are the output of the second latch.

20) The triple redundant latch as in Claim 14 wherein the third latch comprises:

- a) a first PFET, the first PFET having a gate, a drain and a source;
- b) a second PFET, the second PFET having a gate, a drain and a source;
- c) a first NFET, the first NFET having a gate, a drain and a source;
- d) a second NFET, the second NFET having a gate, a drain and a source;
- e) wherein the sources of the first and second PFETs are connected to VDD;
- f) wherein the sources of the first and second NFETs are connected to GND;
- g) wherein the gate of the first NFET, the gate of the first PFET, the drain of the second NFET, and the drain of the second PFET are the input/output of the third latch;
- h) wherein the drain of the first NFET and the drain of the first PFET are connected to the gate of the second NFET, and the gate of the second PFET.

21) The triple redundant latch as in Claim 14 wherein the majority voter comprises:

- a) a first PFET, the first PFET having a gate, a drain and a source;
- b) a second PFET, the second PFET having a gate, a drain and a source;
- c) a third PFET, the third PFET having a gate, a drain and a source;
- d) a first NFET, the first NFET having a gate, a drain and a source;
- e) a second NFET, the second NFET having a gate, a drain and a source;
- f) a third NFET, the third NFET having a gate, a drain and a source;
- g) wherein the source of the first PFET is connected to VDD;
- h) wherein the source of the third NFET is connected to GND;

- i) wherein the drains of the third PFET and the first NFET are connected to the output of the majority voter;
- j) wherein the gates of the second PFET and second NFET are connected to the first input of the majority voter;
- k) wherein the gates of the first PFET and the third NFET are connected to the second input of the majority voter;
- l) wherein the gate of the third PFET is connected to the third input of the majority voter;
- m) wherein the gate of the first NFET is connected to the fourth input of the majority voter;
- n) wherein the drain of the first PFET and the source of the second PFET are connected;
- o) wherein the drain of the second PFET and the source of the third PFET are connected;
- p) wherein the source of the first NFET and the drain of the second NFET are connected;
- q) wherein the source of the second NFET and the drain of the third NFET are connected.

22) A method of manufacturing a triple redundant latch with improved soft error rate comprising:

- a) fabricating a first transfer gate, the first transfer gate having an input, a first control input, a second control input and an output;
- b) fabricating a second transfer gate, the second transfer gate having an input, a first control input, a second control input, and an output;

- c) fabricating a third transfer gate, the transfer third gate having an input, a first control input, a second control input, and an output;
- d) fabricating a first latch, the first latch having an input and an output;
- e) fabricating a second latch, the second latch having an input and an output;
- f) fabricating a third latch, the third latch having an input/output;
- g) fabricating a majority voter, the majority voter having a first input, a second input, a third input, fourth input, and an output;
- h) wherein the input of triple redundant latch is connected to the input of the first transfer gate, the input of the second transfer gate, and the input of the third transfer gate;
- i) wherein a first control input of the triple redundant latch is connected to the first control input of the first transfer gate, the first control input of the second transfer gate, the first control input of the third transfer gate, and the third input to the majority voter;
- j) wherein a second control input of the triple redundant latch is connected to the second control input of the first transfer gate, the second control input of the second transfer gate, the second control input of the third transfer gate, and the fourth input to the majority voter;
- k) wherein the output of the first transfer gate is connected to the input of the first latch;
- l) wherein the output of the second transfer gate is connected to the output of the majority voter, and the input/output of the third latch;
- m) wherein the output of the third transfer gate is connected to the input of the second latch;

- n) wherein the output of the first latch is connected to the first input of the majority voter;
- o) wherein the output of the second latch is connected to the second input of the majority voter.

23) The method of manufacturing a triple redundant latch as in Claim 22 wherein the first transfer gate comprises:

- a) a PFET, the PFET having a gate, a drain and a source;
- b) a NFET, the NFET having a gate, a drain and a source;
- c) wherein the drains of the PFET and the NFET are connected to the input of the first transfer gate;
- d) wherein the sources of the PFET and the NFET are connected to the output of the first transfer gate;
- e) wherein the gate of the NFET is connected to the first control input of the first transfer gate;
- f) wherein the gate of the PFET is connected to the second control input of the first transfer gate.

24) The method of manufacturing a triple redundant latch as in Claim 22 wherein the second transfer gate comprises:

- a) a PFET, the PFET having a gate, a drain and a source;
- b) a NFET, the NFET having a gate, a drain and a source;
- c) wherein the drains of the PFET and the NFET are connected to the input of the second transfer gate;

- d) wherein the sources of the PFET and the NFET are connected to the output of the second transfer gate;
- e) wherein the gate of the NFET is connected to the first control input of the second transfer gate;
- f) wherein the gate of the PFET is connected to the second control input of the second transfer gate.

25) The method of manufacturing a triple redundant latch as in Claim 22 wherein the third transfer gate comprises:

- a) a PFET, the PFET having a gate, a drain and a source;
- b) a NFET, the NFET having a gate, a drain and a source;
- c) wherein the drains of the PFET and the NFET are connected to the input of the third transfer gate;
- d) wherein the sources of the PFET and the NFET are connected to the output of the third transfer gate;
- e) wherein the gate of the NFET is connected to the first control input of the third transfer gate;
- f) wherein the gate of the PFET is connected to the second control input of the third transfer gate.

26) The method of manufacturing a triple redundant latch as in Claim 22 wherein the first latch comprises:

- a) a first PFET, the first PFET having a gate, a drain and a source;
- b) a second PFET, the second PFET having a gate, a drain and a source;

- c) a first NFET, the first NFET having a gate, a drain and a source;
- d) a second NFET, the second NFET having a gate, a drain and a source;
- e) wherein the sources of the first and second PFETs are connected to VDD;
- f) wherein the sources of the first and second NFETs are connected to GND;
- g) wherein the gate of the first NFET, the gate of the first PFET, the drain of the second NFET, and the drain of the second PFET are the input of the first latch;
- h) wherein the drain of the first NFET, the drain of the first PFET, the gate of the second NFET, and the gate of the second PFET are the output of the first latch.

27) The method of manufacturing a triple redundant latch as in Claim 22 wherein the second latch comprises:

- a) a first PFET, the first PFET having a gate, a drain and a source;
- b) a second PFET, the second PFET having a gate, a drain and a source;
- c) a first NFET, the first NFET having a gate, a drain and a source;
- d) a second NFET, the second NFET having a gate, a drain and a source;
- e) wherein the sources of the first and second PFETs are connected to VDD;
- f) wherein the sources of the first and second NFETs are connected to GND;
- g) wherein the gate of the first NFET, the gate of the first PFET, the drain of the second NFET, and the drain of the second PFET are the input of the second latch;
- h) wherein the drain of the first NFET, the drain of the first PFET, the gate of the second NFET, and the gate of the second PFET are the output of the second latch.

28) The method of manufacturing a triple redundant latch as in Claim 22 wherein the third latch comprises:

- a) a first PFET, the first PFET having a gate, a drain and a source;
- b) a second PFET, the second PFET having a gate, a drain and a source;
- c) a first NFET, the first NFET having a gate, a drain and a source;
- d) a second NFET, the second NFET having a gate, a drain and a source;
- e) wherein the sources of the first and second PFETs are connected to VDD;
- f) wherein the sources of the first and second NFETs are connected to GND;
- g) wherein the gate of the first NFET, the gate of the first PFET, the drain of the second NFET, and the drain of the second PFET are the input/output of the third latch;
- h) wherein the drain of the first NFET and the drain of the first PFET are connected to the gate of the second NFET and the gate of the second PFET.

29) The method of manufacturing a triple redundant latch as in Claim 22 wherein the majority voter comprises:

- a) a first PFET, the first PFET having a gate, a drain and a source;
- b) a second PFET, the second PFET having a gate, a drain and a source;
- c) a third PFET, the third PFET having a gate, a drain and a source;
- d) a first NFET, the first NFET having a gate, a drain and a source;
- e) a second NFET, the second NFET having a gate, a drain and a source;
- f) a third NFET, the third NFET having a gate, a drain and a source;
- g) wherein the source of the first PFET is connected to VDD;
- h) wherein the source of the third NFET is connected to GND;

- i) wherein the drains of the third PFET and the first NFET are connected to the output of the majority voter;
- j) wherein the gates of the second PFET and second NFET are connected to the first input of the majority voter;
- k) wherein the gates of the first PFET and the third NFET are connected to the second input of the majority voter;
- l) wherein the gate of the third PFET is connected to the third input of the majority voter;
- m) wherein the gate of the first NFET is connected to the fourth input of the majority voter;
- n) wherein the drain of the first PFET and the source of the second PFET are connected;
- o) wherein the drain of the second PFET and the source of the third PFET are connected;
- p) wherein the source of the first NFET and the drain of the second NFET are connected;
- q) wherein the source of the second NFET and the drain of the third NFET are connected.

30) A triple redundant latch for reducing soft errors comprising:

- a) a first means for setting and retaining a logical value;
- b) a second means for setting and retaining a logical value;
- c) a third means for setting and retaining a logical value;
- d) a means for setting a logical value into the third means for setting and retaining a logical value determined by inputs provided by the first and

second means for setting and retaining a logical value, and control used to set the means for setting and retaining a logical value;

- e) wherein an identical logic value is set in each means for setting and retaining a logical value;
- f) wherein a propagation delay through the third means for setting and retaining a logical value is the only propagation delay of the triple redundant latch.